25MHz RRIO Operational Amplifiers (Single)

Description

The SL9061 is a single channel low voltage (1.5V to 5.5V) operational amplifiers (opamps) with rail-to-rail input and output swing capabilities. These devices are very suitable for applications where low voltage operation, a small footprint, and high capacitive load drive are required.

Features

- Excellent THD+N 100dB
- Excellent SNR 110dB
- Rail-to-rail input and output
- Low input offset voltage: ±0.5mV typ
- Unity-gain bandwidth: 25MHz
- Low quiescent current: 800μA typ
- Operational at supply voltages as low as 1.5V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance

Applications

- Infotainment system
- HVAC: heating, ventilating, and air conditioning
- Motor control
- Wearable devices
- Sensor signal conditioning
- Power modules
- Active filters

Table 1 Device Summary

Order code	Package	Packing
SL9061A	SOT23-5	Reel
SL9061B	SOT23-5	Reel

SOT23-5

1 Block Diagram and Application Circuit

Figure 1 Block Diagram

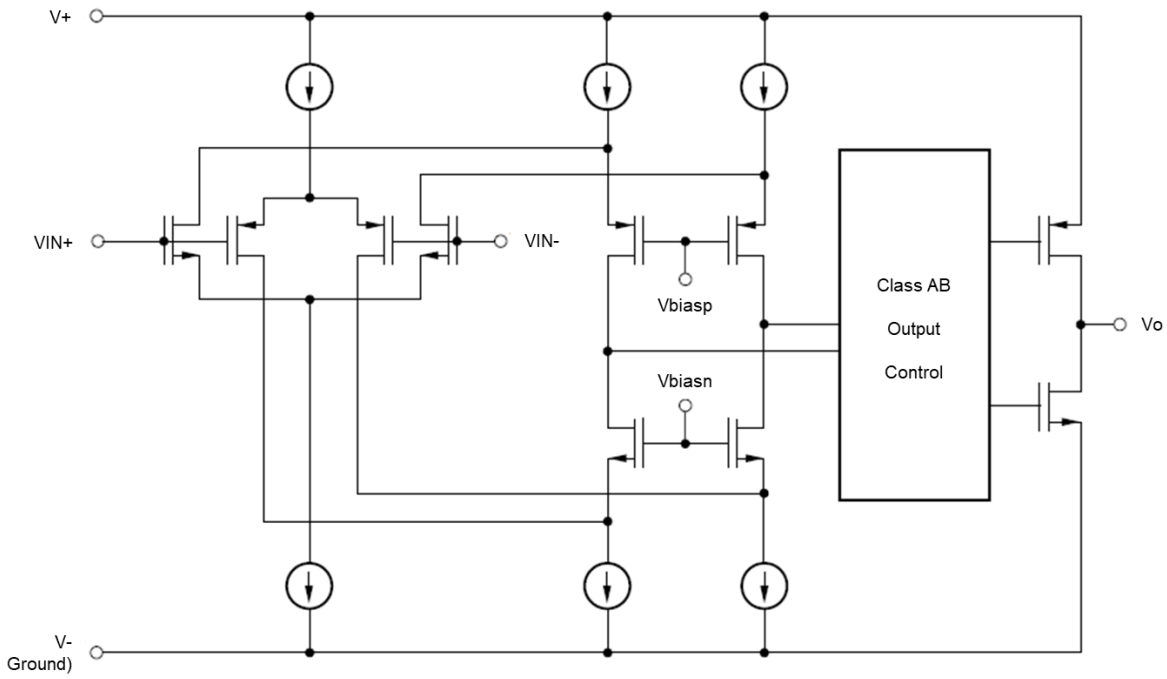
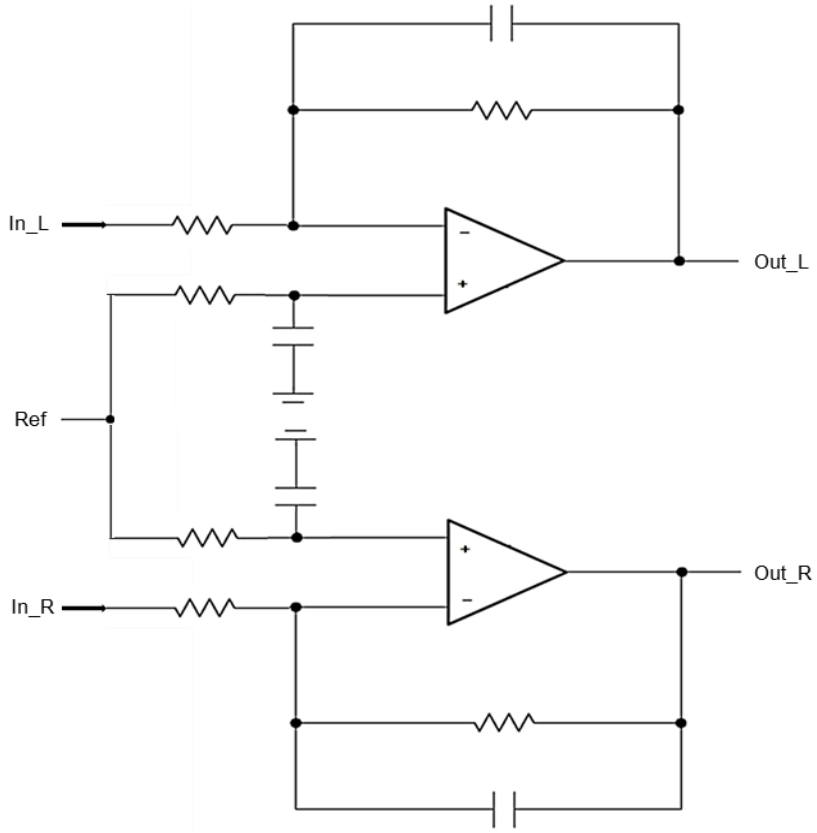


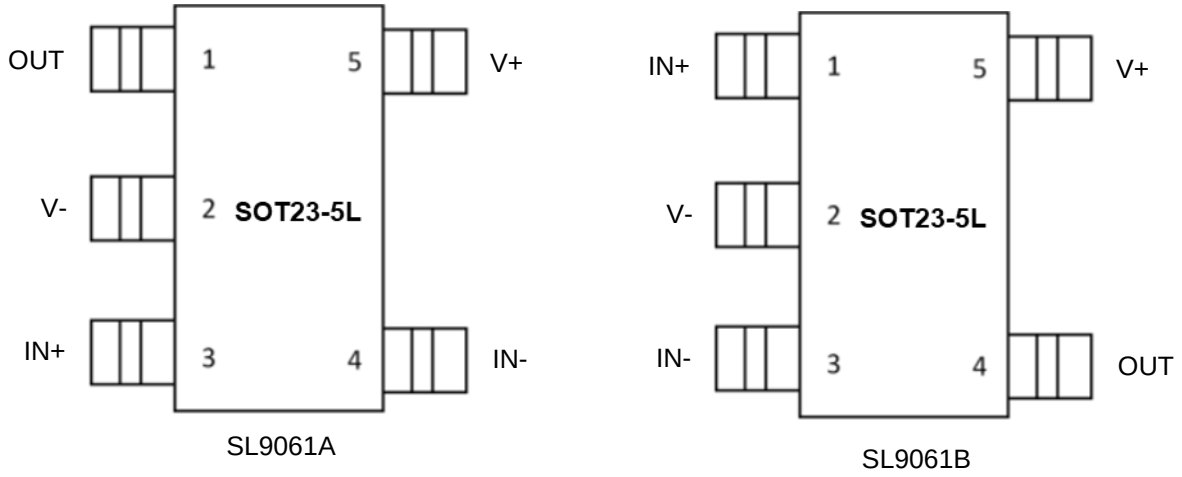
Figure 2 Typical Application Circuit **(Stereo Sound Input Amplifier)**



2 Pin Description

2.1 SL9061A/B Pinouts

Figure 3 SL9061A/B Pinouts



Pin number	Pin name	Description
1	OUT	Output
2	V-	Negative supply or ground
3	IN+	Non-inverting input
4	IN-	Inverting input
5	V+	Positive supply

Pin number	Pin name	Description
1	IN+	Non-inverting input
2	V-	Negative supply or ground
3	IN-	Inverting input
4	OUT	Output
5	V+	Positive supply

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vs	Supply voltage (V+) - (V-)	-0.3 to +6	V
IN+, IN-	Input pin voltage	(V-) - 0.5 to (V+) +0.5	V
OUT	Output pin voltage	(V-) - 0.5 to (V+) +0.5	V
Tj	Junction temperature	150	°C
Tstg	Storage temperature	-55 to +150	°C

3.2 Thermal Data

Table 3 Thermal Data

Package	Rth j-amb	Rth j-case	Unit
SOT23-5	184	100	°C/W

3.3 ESD and Latch Up

Table 4 ESD and Latch up

Symbol	Parameter	Value	Unit
All pins	ESD (HBM) ESD (CDM)	±6,000 ±500	V V

3.4 Electrical Characteristics

For Vs = (V+) - (V-) = 5V at Ta = 25°C, RL = 10kΩ connected to Vs/2, Vcm = Vs/2, and Vout = Vs/2 (unless otherwise noted).

Table 5 Electrical Characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vs	Supply voltage (V+) - (V-)		1.5		5.5	V
Ta	Operating ambient temperature		-40		125	°C
Power Supply						
Iq	Quiescent current per amplifier	Vs=5.5V, Io=0mA		800		μA
		all temp			900	
Offset Voltage						
Vos	Input offset voltage			±0.5	±2.0	mV
		all temp			±3.0	mV
dVos/dT	Drift	all temp		±0.5		μV/°C
PSRR	Power-supply rejection ratio	At DC		100		dB
Csep	Channel separation	At DC		120		dB
Input Voltage Range						
Vcm	Common mode voltage range	Vs=1.5V to 5V	(V-)-0.1		(V+)+0.1	V
CMRR	Common mode rejection ratio	At DC		100		dB
Input Bias Current						
Ib	Input bias current			±0.5		pA
Ios	Input offset current			±0.05		pA
Noise						
En	Input voltage noise	f=20Hz to 20kHz		1.5		μV
en	Input voltage noise density	f=10kHz		7		nV/√Hz
		f=1kHz		15		
Input Capacitance						
Cid	Differential			2		pF
Cic	Common mode			4		pF
Open Loop Gain						
Aol	Open loop voltage gain			110		dB
Frequency Response						
GBP	Gain bandwidth product	G=+1, CL=10pF		25		MHz
φ	Phase margin	G=+1, CL=10pF		60		°
Cload	Capacitive load	G=+1			1	nF
SR	Slew rate	G=+1, CL=100pF		8		V/μs

Ts	Settling time	To 0.1%, 2V step, G=+1, CL=100pF		0.5		μs
Tor	Overload recovery time	VIN x gain > Vs, CL=100pF		50		ns
THD+N	Total harmonic distortion + Noise (3rd order filter; BW= 80kHz at -3dB.)	Vs=5.5V, Vcm=2.5V, Vo=1Vrms, G=+1, f=1kHz		100		dB
SNR	Signal to Noise Ratio			110		dB
Output						
Vo	Voltage output swing from supply rails	RL=10kΩ		5	10	mV
		RL=2kΩ		15	30	
Isc	Short circuit current			±50		mA
Zo	Open loop output impedance	f=10MHz		100		Ω

3.5 Typical Electrical Characteristics

Figure 4 Vos Distribution

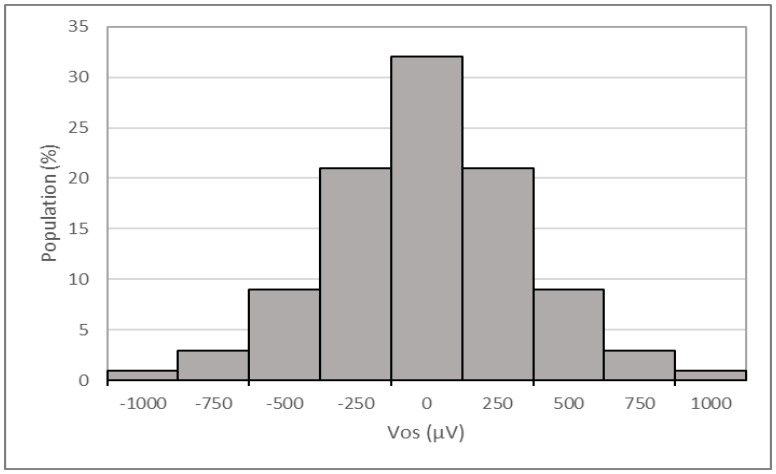


Figure 5 Vos vs Input Common Mode Voltage

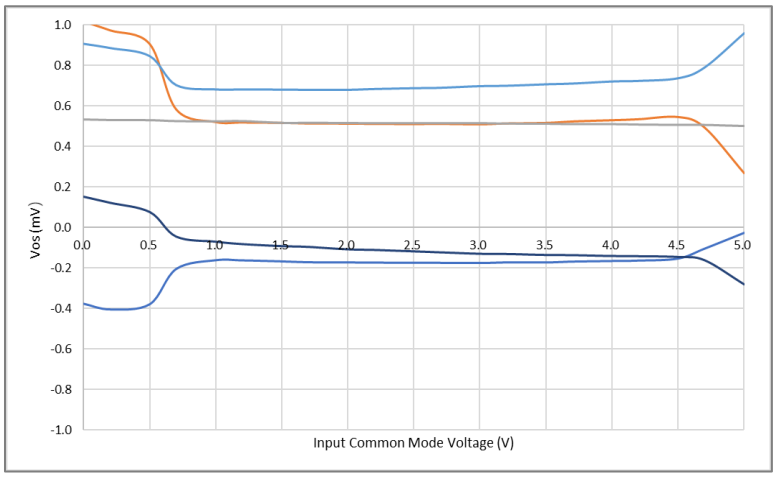


Figure 6 Vos vs

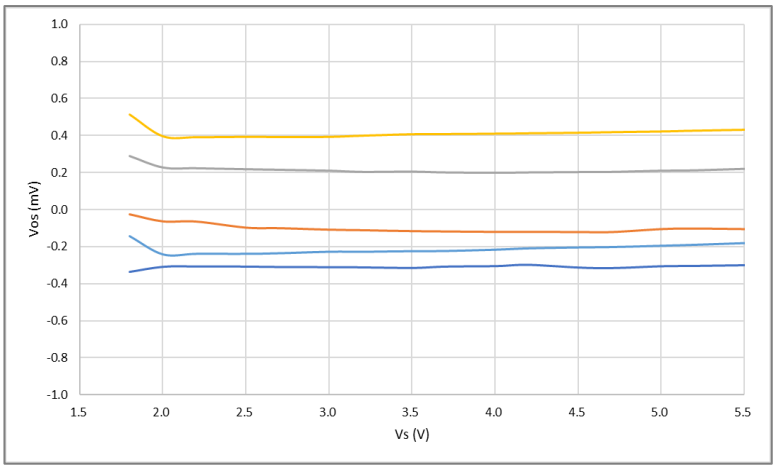


Figure 7 THD+N vs Frequency

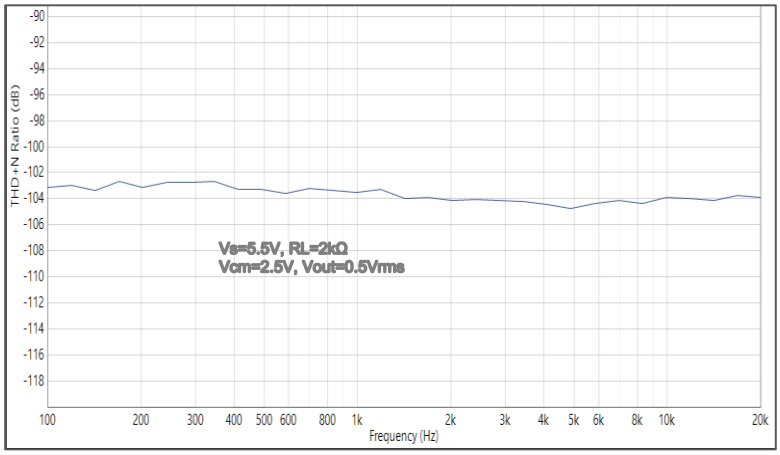


Figure 8 Large Signal Step Response

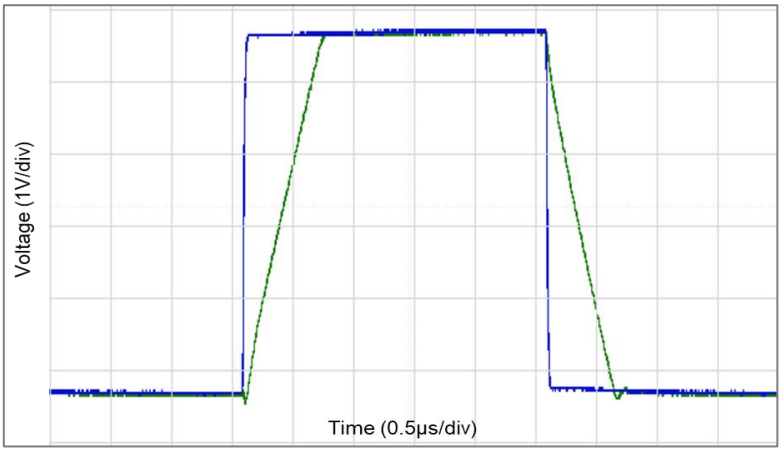
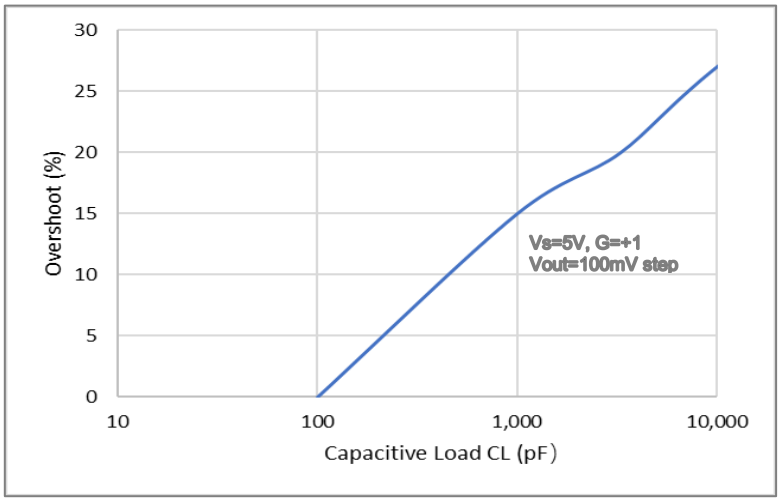


Figure 9 Small Signal Overshoot vs Capacitive Load



4 Functional Description

4.1 Overview

The SL 9061 device is a low power, rail-to-rail input and output opamp. The device operates from 1.5V to 5.5V, is unity gain stable, and designed for a wide range of applications and used in virtually any single supply application.

4.2 Rail to Rail Input

The input common mode voltage range of the SL 9061 extends 100mV beyond the supply rails for the full supply voltage range of 1.5V to 5.5V. This performance is achieved with a complementary input stage: a N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 1. The N-channel pair is active for input voltages close to the positive rail, typically (V+)-1.4V to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately (V+)-1.4V. There is a transition region, in which both pairs are on. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

4.3 Rail to Rail Output

Designed as a low power, low voltage operational amplifier, the SL 9061 delivers a robust output drive capability. A class AB output stage with common source Mosfets achieves full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 10mV (typ) of either supply rail, regardless of the applied power supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

4.4 Overload Recovery

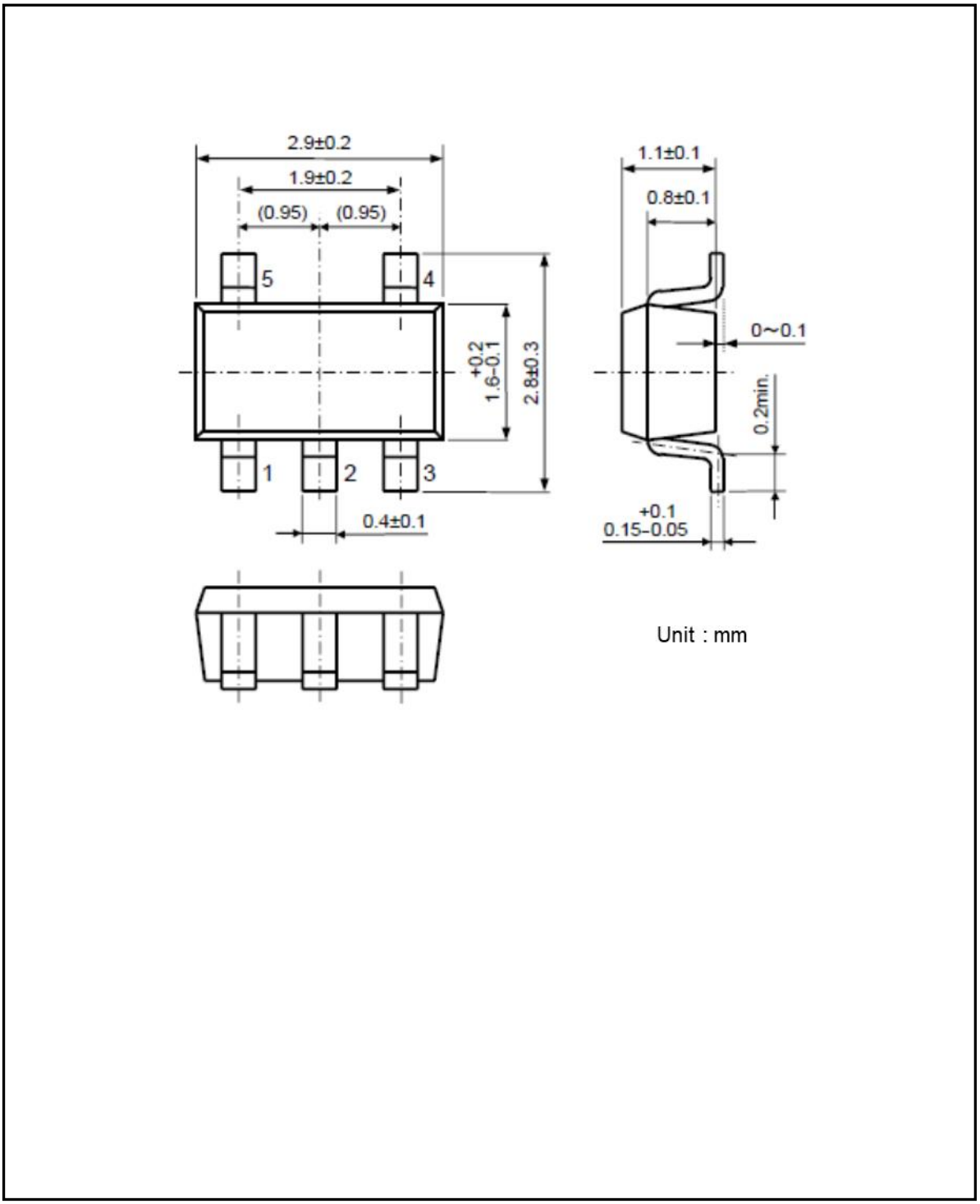
Overload recovery is defined as the time required for the opamp output to recover from a saturated state to a linear state. The output devices of the opamp enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. The overload recovery time for the SL 9061 is approximately 300ns.

4.5 EMI Rejection

The SL 9061 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components.

5 Package Information

Figure 10 SOT23-5 Mechanical Data and Package Dimensions



6 Packing Information

Figure 12 Reel Packing Information